HMC629LP4 / 629LP4E

v02.0108

3 dB LSB GaAs MMIC 4-BIT DIGITAL ATTENUATOR, DC - 6 GHz

Typical Applications

The HMC629LP4(E) is ideal for:

- Cellular/3G Infrastructure
- WiBro / WiMAX / 4G
- Microwave Radio & VSAT
- Test Equipment and Sensors
- IF & RF Applications

Features

3 dB LSB Steps to 45 dB

Power-Up State Selection

Low Insertion Loss: 2.5 dB

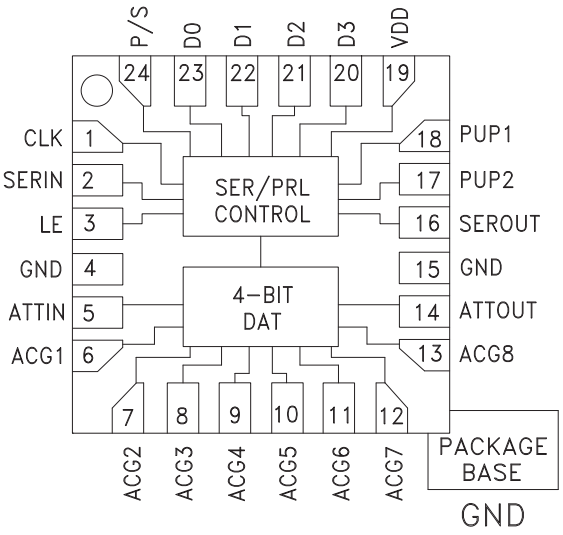
TTL/CMOS Compatible, Serial, Parallel or Latched Parallel Control

±0.25 dB Typical Step Error

Single +3V or +5V Supply

24 Lead 4x4mm SMT Package: $16mm^2$

Functional Diagram



General Description

The HMC629LP4(E) is a broadband 4-bit GaAs IC Digital Attenuator in a low cost leadless SMT package. This versatile digital attenuator incorporates off-chip AC ground capacitors for near DC operation, making it suitable for a wide variety of RF and IF applications. The dual mode control interface is CMOS/TTL compatible, and accepts either a three wire serial input or a 4-bit parallel word. For applications which require only 33 dB of attenuation range, the HMC629LP4(E) provides excellent attenuation accuracy up to 10 GHz. The HMC629LP4(E) is housed in a RoHS compliant 4x4 mm QFN leadless package, and requires no external matching components.

Electrical Specifications, T_A = +25° C, 50 Ohm System, with Vdd = +5V & Vctl = 0/+5V (Unless Otherwise Noted)

Parameter	Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss	DC - 6		2.5	5	dB dB
Attenuation Range	DC - 6		45		dB
Return Loss (ATTIN, ATTOUT, All Atten. States)	DC - 6		17		dB
Attenuation Accuracy: (Referenced to Insertion Loss) All Attenuation States		± (0.50 + 5% of Atten. Setting) Max.			dB dB

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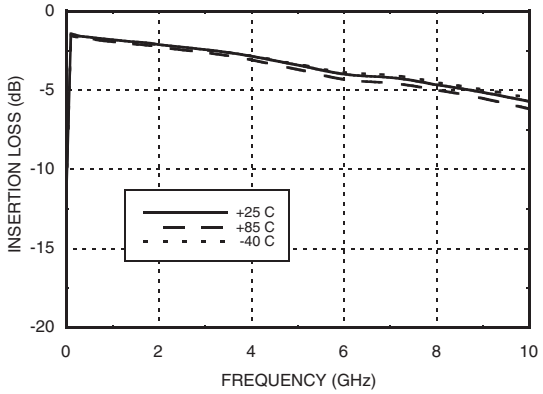
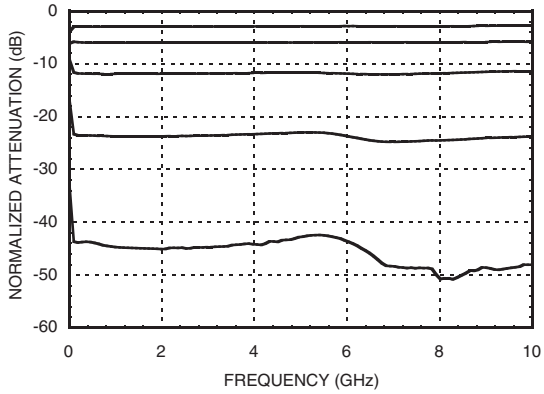
Insertion Loss vs. Temperature



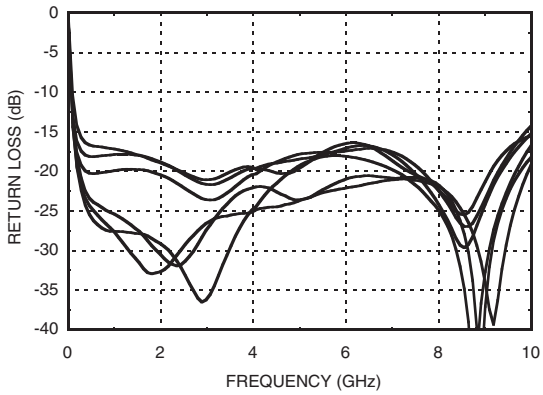
Normalized Attenuation

(Only Major States are Shown)



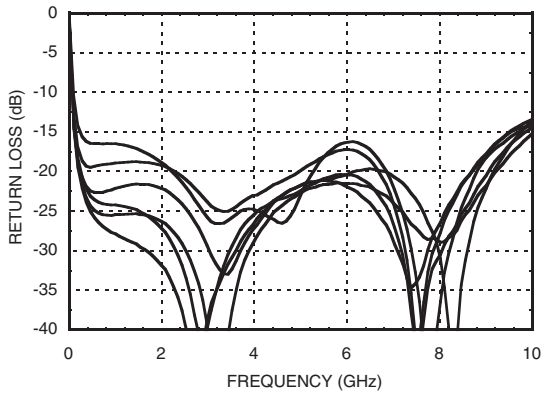
Input Return Loss

(Only Major States are Shown)

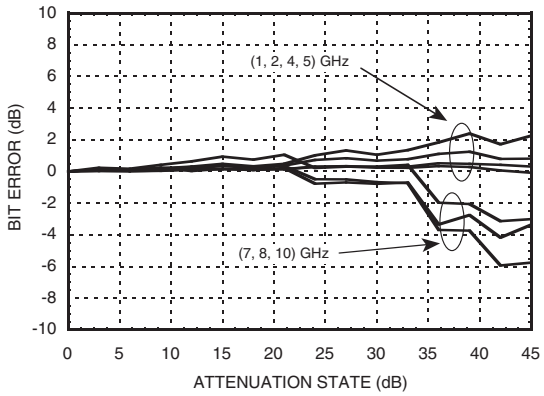


Output Return Loss

(Only Major States are Shown)

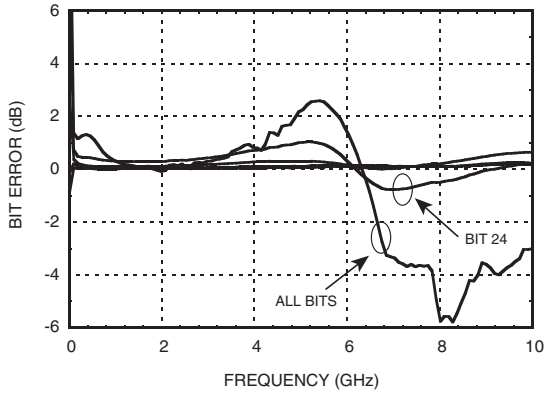


Bit Error vs. Attenuation State



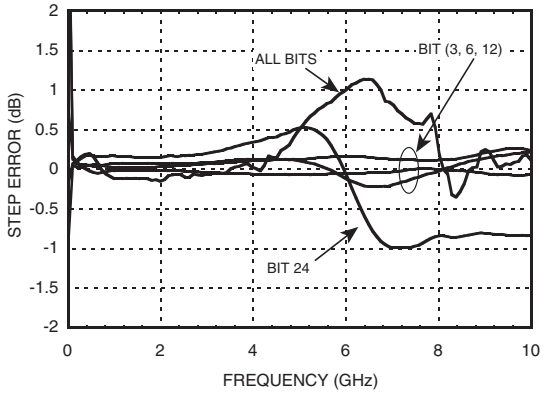
Bit Error vs. Frequency

(Only Major States are Shown)

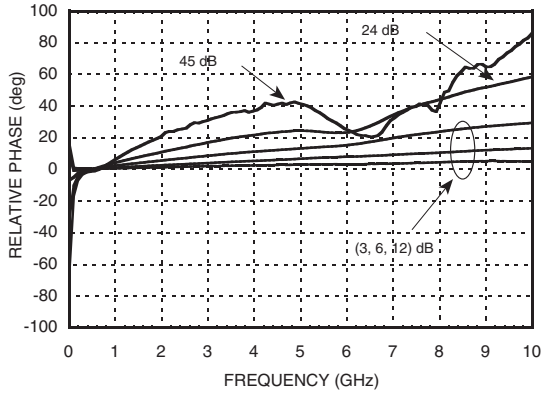


Step Error vs. Frequency

(Only Major States are Shown)

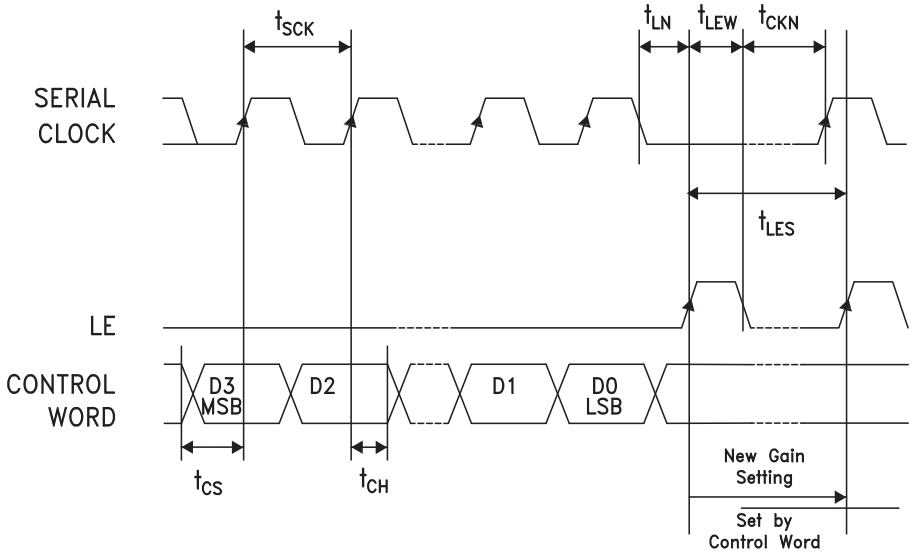


Normal Relative Phase vs. Frequency



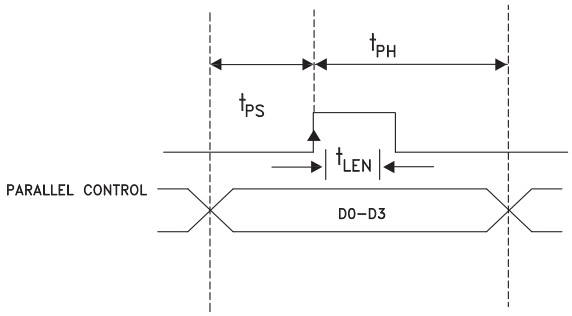
Serial Control Interface

The serial control interface is enabled when the P/S pin is at logic 1. The 4-bit control word is entered MSB first, on each positive-going clock edge. After the fourth clock pulse, the control word is latched in on the positive-going edge of LE pulse. The newest attenuation setting will be invoked at the same moment the control word is latched in.



Parameter	Typ.
Min. serial period, t_{SCK}	100 ns
Control set-up time, t_{CS}	20 ns
Control hold-time, t_{CH}	20 ns
LE hold-time, t_{LN}	10 ns
Min. LE pulse width, t_{LEW}	10 ns
Min LE pulse spacing, t_{LES}	430 ns
Serial clock hold-time from LE, t_{CKN}	10 ns

Timing Diagram (Latched Parallel Mode)



Parallel Mode (Direct Parallel Mode & Latched Parallel Mode)

Note: The parallel mode is enabled when P/S is set to low.

Direct Parallel Mode - The attenuation state is changed by the Control Voltage Inputs directly. The LE (Latch Enable) must be at a logic high to control the attenuator in this manner.

Latched Parallel Mode - The attenuation state is selected using the Control Voltage Inputs and set while the LE is in the Low state. The attenuator will not change state while LE is Low. Once all Control Voltage Inputs are at the desired states the LE is pulsed. See timing diagram below for reference.

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Power-Up States

The Power-up (PUP) states work in both serial and parallel modes, provided that LE is held low. The DVGA latches in the state of the D3-D0 pins 200 ms after power-up. The state of D3-D0 pins should be held firmly high or low for at least 250 ms following power-up. The PUP state is locked out after the first LE pulse, until Vdd drops below 4.5 V.

PUP Truth Table

LE	PUP1	PUP2	Attenuation State
0	0	0	45 dB
0	1	0	45 dB
0	0	1	45 dB
0	1	1	I. L.
1	X	X	0 to 45 dB

Note: Power-Up with LE= 1 provides direct parallel operation and D0 - D3, and PUP1 and PUP2 are not used.

Absolute Maximum Ratings

RF Input Power (DC - 6 GHz) [1]	27 dBm (T = +85 °C)
Digital Inputs (Data, Shift Clock, Latch Enable & Serial Input)	-1.5V to (Vdd +1.5V) Vdc
Bias Voltage (Vdd)	5.6 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 9.8 mW/°C above 85 °C) [1]	0.635 W
Thermal Resistance	102 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

[1] At max gain settling

Truth Table

Control Voltage Input				Attenuation State
D3	D2	D1	D0	
High	High	High	High	Reference I.L.
High	High	High	Low	3 dB
High	High	Low	High	6 dB
High	Low	High	High	12 dB
Low	High	High	High	24 dB
Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.				

Bias Voltage

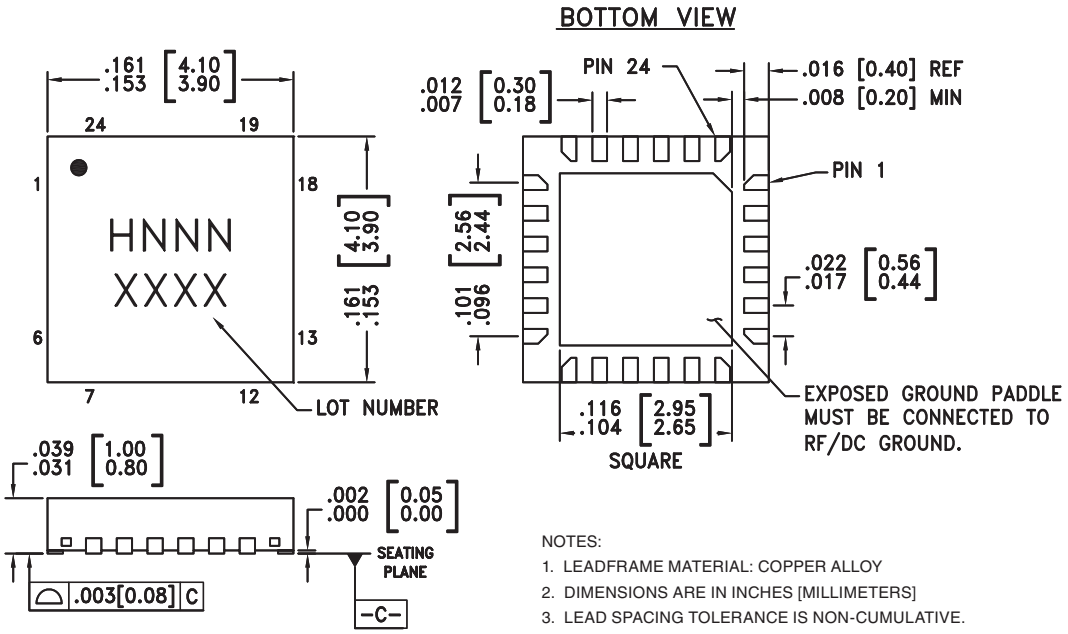
Vdd (Vdc)	Idd (Typ.) (mA)
5	2.0

TTL/CMOS Control Voltage

State	Vdd= +3V or +5V
Low	0 to 0.8V
High	2.0V to Vdd

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

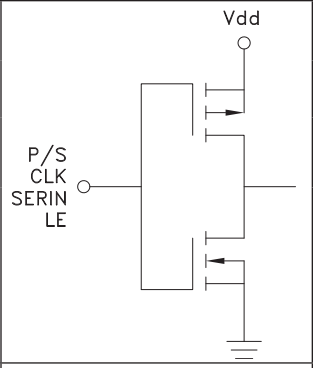
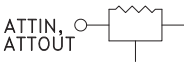
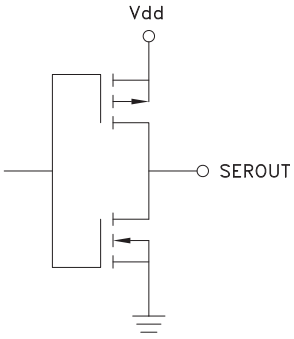
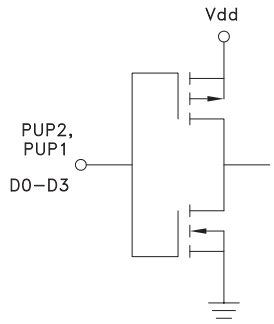
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO PCB DESIGN AND ASSEMBLY FOR QFN PACKAGES APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

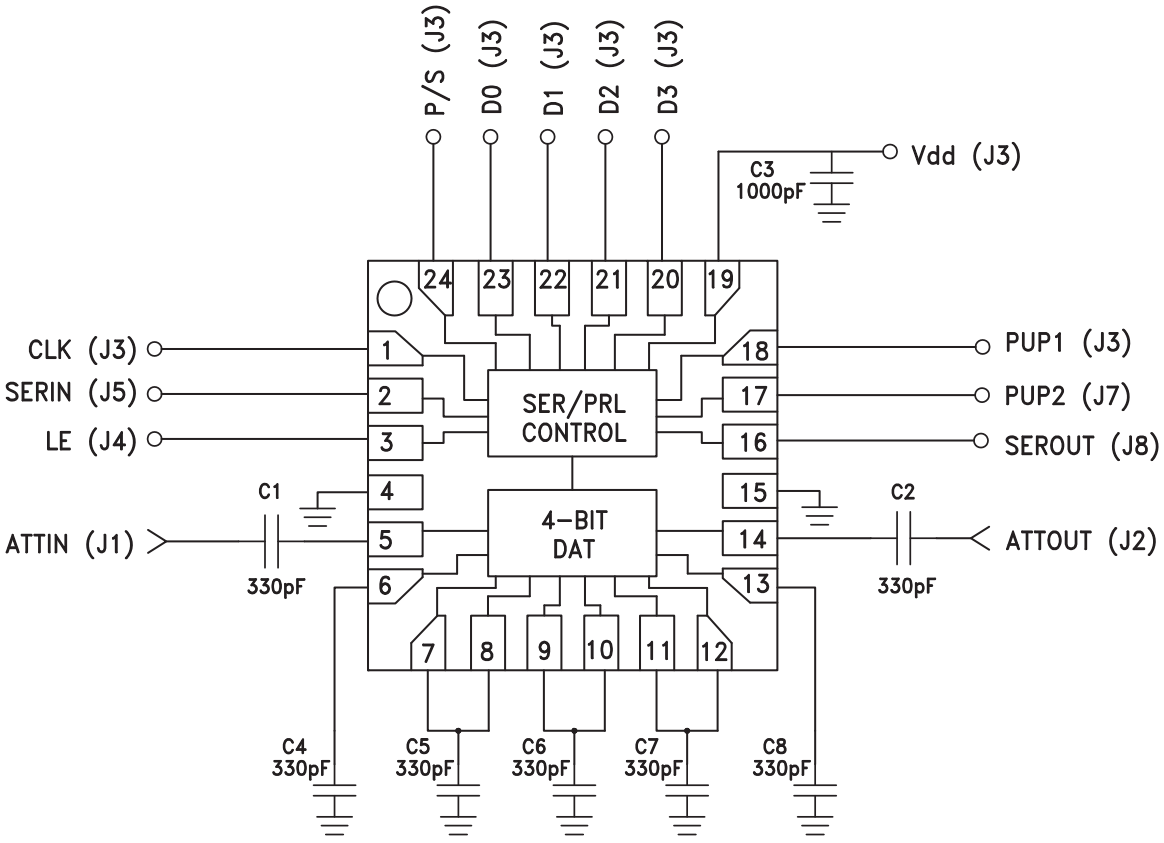
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC629LP4	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H629 XXXX
HMC629LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H629 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

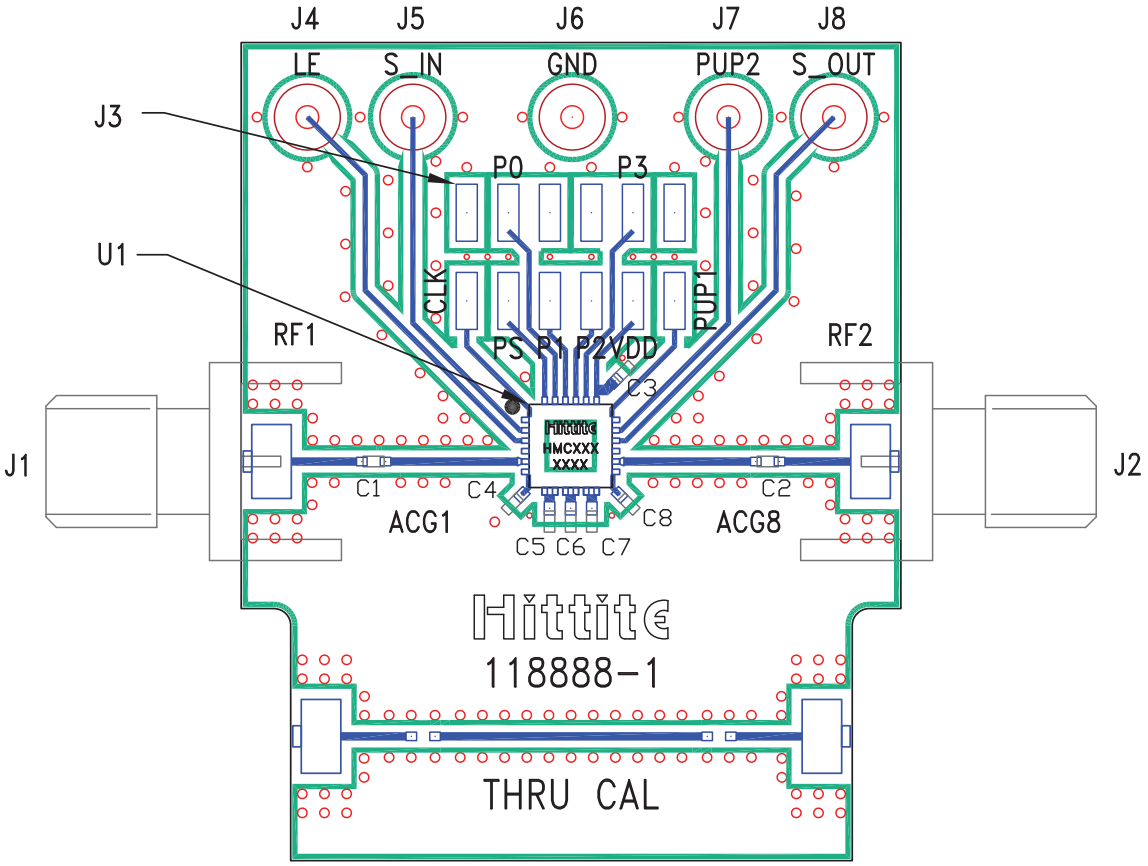
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
24	P/S	See truth table, control voltage table and timing diagram.	
1	CLK		
2	SERIN		
3	LE		
4, 15	GND	These pins and package bottom must be connected to RF/DC ground.	
5, 14	ATTIN, ATTOUT	These pins are DC coupled and matched to 50 Ohms. Blocking capacitors are required. Select value based on lowest frequency of operation.	
6 - 13	ACG1 - ACG6	External capacitors to ground are required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible. See Application Circuit.	
16	SEROUT	Serial input data delayed by 6 clock cycles.	
17, 18	PUP2, PUP1	See truth table, control voltage table and timing diagram.	
20 - 23	D3, D2, D1, D0		
19	Vdd	Supply voltage	

Application Circuit



Evaluation PCB



List of Materials for Evaluation PCB 118889 [1]

Item	Description
J1 - J2	PCB Mount SMA Connector
J3	12 Pin DC Connector
J4 - J8	DC Pin
C1 - C2	100 pF, capacitor 0402 pkg
C3	1000 pF, capacitor 0402 pkg
C4 - C8	330 pF, capacitor 0402 pkg
U1	HMC624LP4(E) Digital Attenuator
PCB [2]	118888 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Notes: